

# **IEEE-2010 PROJECTS**

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### **VLSI**

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# VLSI

TECHNOLOGY: VLSI

DOMAIN: CORE VLSI

| S.NO | PROJECT CODE | PROJECT TITLES  | DESCRIPTION  | YEAR |
|------|--------------|---|--|------|
| 1.   | ITVL01       | Novel Area-Efficient FPGA Architectures For Fir Filtering With Symmetric Signal Extension | This paper presents four novel area-efficient field-programmable gate-array (FPGA) bit-parallel architectures of finite impulse response (FIR) filters that smartly support the technique of symmetric signal extension while processing finite length signals at their boundaries.  | 2009 |
| 2.   | ITVL02       | A Fast VLSI Design Of Sms4 Cipher Based On Twisted BDD S-Box Architecture                 | SMS4 is a 128-bit block cipher used in the WAPI standard for protecting data packets in WLAN. In this paper, various S-box circuit architectures were evaluated firstly and the twisted BDD with $m=4$ was proved as the fastest one. A fast SMS4 cipher VLSI implementation was completed based on the twisted BDD S-box architecture | 2009 |
| 3    | ITVL03       | Power optimization of linear feedback shift Register (LFSR) for low power BIST            | This paper proposes a low power Linear Feedback Shift Register (LFSR) for Test Pattern Generation (TPG) technique with reducing power dissipation during testing.  | 2009 |
| 4.   | ITVL04       | Fault Secure Encoder And Decoder For Nano-memory Applications                             | This paper proposed the encoder and decoder circuitry around the memory blocks have become susceptible to soft errors as well and must also be protected. We introduce a new approach to design fault-secure encoder and decoder circuitry for memory designs.   | 2009 |

|    |        |   |  |      |
|----|--------|---|--|------|
| 5. | ITVL05 | Hardware Algorithm For Variable Precision Multiplication On FPGA                          | A hardwired algorithm for computing the variable precision multiplication is presented in this paper. The computation method is based on the use of a parallel multiplier .Our architecture has been tailored to use these efficient resources and the resulting architecture is dedicated to compute the multiplication of operands of sizes ranging from 1×64 bits to 64× 64 bits.                         | 2009 |
| 6. | ITVL06 | Low-Power Leading-Zero Counting And Anticipation Logic For High-Speed Floating Point Unit | In this paper, a new leading-zero counter (or detector) is presented. New Boolean relations for the bits of the leading-zero count are derived that allow their computation to be performed using standard carry-look ahead techniques. Using the proposed approach various design choices can be explored and different circuit topologies can be derived for the design of the leading-zero counting unit. | 2009 |
| 7. | ITVL07 | Asynchronous Computing in Sense Amplifier-Based Pass Transistor Logic                     | The dual-rail handshaking protocol. The proposed self-timed SAPTL architectures provide robust and efficient asynchronous computation using a glitch-free protocol to avoid possible dynamic timing hazards. Simulation and measurement results show that the self-timed SAPTL with dual-rail protocol exhibits energy-delay characteristics better than synchronous and bundled data self-timed approaches  | 2009 |

## TECHNOLOGY: VLSI

## DOMAIN: IMAGE PROCESSING

| S.NO | PROJECT CODE | PROJECT TITLES  | DESCRIPTION  | YEAR |
|------|--------------|---|--|------|
| 8    | ITVL08       | Asynchronous Protocol Converters for Two-Phase Delay-Insensitive Global Communication | As system-level interconnect incurs increasing penalties in latency, round-trip cycle time and power, and as timing-variability becomes an increasing design challenge,This paper proposes two new | 2009 |

|    |        |  |   |      |
|----|--------|--|---|------|
|    |        |  | architecture for a family of asynchronous protocol converters that translate between two- and four-phase protocols, thus facilitating robust system design using efficient global two-phase communication and local four-phase computation.   |      |
| 9. | ITVL09 | Design and Implementation of a Field Programmable CRC Circuit Architecture                       | The design and implementation of a programmable cyclic redundancy check (CRC) computation circuit architecture, suitable for deployment in network related system-on-chips (SoCs) is presented. The architecture has been designed to be field reprogrammable so that it is fully flexible in terms of the polynomial deployed and the input port width. The circuit includes an embedded configuration controller that has a low reconfiguration time and hardware cost.                               | 2009 |
| 10 | ITVL10 | Exploiting Memory Soft Redundancy for Joint Improvement of Error Tolerance And Access Efficiency | In this paper, we propose to exploit the inherent memory <i>soft (transient) redundancy</i> for on-chip memory design. Due to the mismatch between fixed cache line size and runtime variations in memory spatial locality, many irrelevant data are fetched into the memory thereby wasting memory spaces. The proposed soft-redundancy allocated memory detects and utilizes these memory spaces for jointly achieving efficient memory access and effective error control. A runtime reconfiguration | 2009 |

**TECHNOLOGY: VLSI**

**DOMAIN: DIGITAL SYSTEM DESIGN**

| S.NO | PROJECT CODE | PROJECT TITLES  | DESCRIPTION  | YEAR |
|------|--------------|---|--|------|
| 11   | ITVL11       | Soft-Error Tolerance and Mitigation in Asynchronous Burst-Mode Circuits | The proposed method is more robust and less expensive than the typical triple modular redundancy error tolerance method and often even less expensive than previously proposed concurrent error detection methods, which only provide detection but no correction. The second solution is an error mitigation approach, which leverages a newly devised soft-error | 2009 |

|            |               |  |  |      |
|------------|---------------|--|--|------|
|            |               |  | susceptibility assessment method for ABMMs, along with partial duplication, to suppress a carefully chosen subset of transient errors..  |      |
| <b>12</b>  | <b>ITVL12</b> | Design of Network-on-Chip Architectures with a Genetic Algorithm-Based Technique                   | Networks on chips (NoCs) are becoming popular as they provide a solution for the interconnection problems on large integrated circuits (ICs). But even in a NoC, link-power can become unacceptably high and data rates are limited when conventional data transceivers are used. In this paper, we present a low-power, high-speed source-synchronous link transceiver which enables a reduction in link power together with an 80% increase in data-rate. reliability .  | 2009 |
| <b>13.</b> | <b>ITVL13</b> | Efficient On-Chip Crosstalk Avoidance CODEC Design   | Interconnect delay has become a limiting factor for circuit performance in deep sub-micrometer designs. As the crosstalk in an on-chip bus is highly dependent on the data patterns transmitted on the bus, different crosstalk avoidance coding schemes have been proposed to boost the bus speed and/or reduce the overall energy consumption. Despite the availability of the codes, no systematic mapping of data words to code words has been proposed for CODEC design.  | 2009 |
| <b>14.</b> | <b>ITVL14</b> | Fast Enhancement of Validation Test Sets for Improving the Stuck-at Fault Coverage of RTL Circuits | A digital circuit usually comprises a controller and data path. The time spent for determining a valid controller behaviour to detect a fault usually dominates test generation time. In this paper, we present a novel methodology wherein the controller behaviours exercised by test sequences in a validation test set are reused for detecting faults in the data path  | 2009 |
| <b>15.</b> | <b>ITVL15</b> | Efficient Communication Between the Embedded Processor and the Reconfigurable Logic on an FPGA     | Increasing device densities have prompted FPGA manufacturers, such as Xilinx and Altera, to incorporate larger embedded components, including multipliers, DSP blocks and even embedded processors. One of the recent architectural enhancements in the Xilinx Virtex family architecture is the introduction of the PowerPC405 hard-core embedded processor. In this paper we present a Software Defined Radio application that serves as a vehicle for investigating effective communication between the PowerPC405 processor and the surrounding FPGA fabric. | 2009 |

|           |               |   |  |      |
|-----------|---------------|---|--|------|
| <b>16</b> | <b>ITVL16</b> | FPGA implementation of 32 bit ECOMIPS CPU IP core | MIPS is nothing but a Microprocessor without Interlocked Pipeline Stages. The main aim of the project is to develop an IP core for MIPS architecture. Here we developed a VHDL code for each block of MIPS architecture and combined all the blocks using Top-level design. We verify each block functionally using ISE simulator and finally verify the top level design. After simulation we can synthesize and finally generate bit file using Xilinx 9.1 synthesis tool. | 2008 |
|-----------|---------------|---|--|------|

## TECHNOLOGY: VLSI

### DOMAIN: TESTING

| S.NO       | PROJECT CODE  | PROJECT TITLES  | DESCRIPTION   | YEAR |
|------------|---------------|---|---|------|
| <b>17.</b> | <b>ITVL17</b> | Design and Implementation of WI-FI MAC Transmitter using VHDL | Wireless communication is one of the fastest growing technologies. The demand for connecting devices without cable is increasing everywhere. Wireless Local Area Networks (WLAN) can connect roaming devices to the Internet. At home, a wireless LAN can connect roaming devices to the internet. Wireless devices are both popular and cost effective and have considered interest from the industry and academia. Users of wireless networks either, walking on the streets, driving a car, or operating a portable computer on an aircraft, enjoy the exchange of information without worrying about how technology makes such exchange possible. | 2009 |
| <b>18.</b> | <b>ITVL18</b> | A VHDL implementation of UART with BIST capability            | This project mainly focuses on the design of UART with embedded BIST capability and on the problems of Very Large Scale Integrated (VLSI) testing followed by the behavior of UART circuit using Very High Speed Integrated Hardware In the implementation phase, the BIST technique will be incorporated into the UART design before the overall design is synthesized by means of reconfiguring the   | 2009 |

|            |               |   |  |      |
|------------|---------------|---|--|------|
|            |               |   | existing design to match testability requirements  |      |
| <b>19.</b> | <b>ITVL19</b> | AMBA AHB Bus Potocol Checker with Efficient Debugging Mechanism | <p>Use of IPs plays a very vital role in the shortening the design cycle and thus, the time to market of socs. The communication between the integrated IPs is enabled by a common, shared on chip bus. The behavior of the bus becomes vital to the working of the soc.</p> <p>We propose an efficient rule based bus protocol debugging mechanism which uses an error reference table that helps in achieving higher efficiency over traditional simulation based bus protocol monitors.</p> | 2008 |
| <b>20.</b> | <b>ITVL20</b> | CRYPTOGRAPHY CORE   | The continuous increase in demand for security in electronic systems and communication systems which lacks a secure architecture has resulted in the need to provide an cryptography architecture with high secure core.This proposed architecture implements three symmetric algorithms namely the standard AES, standard DES and proposed modified DES(MMDV) algorithms.   | 2009 |

## TECHNOLOGY: VLSI

## DOMAIN: COMMUNICATION

| S.NO       | PROJE<br>CT<br>CODE | PROJECT TITLES   | DESCRIPTION  | YEAR |
|------------|---------------------|--|--|------|
| <b>21.</b> | <b>ITVL21</b>       | The iieee1394 high-speed serial bus provides a fast, scalable, easy-to-use digital interface for throughput intensive consumer electronics devices | <p>The IEEE1394 High-Speed Serial Bus provides a fast, scalable, easy-to-use digital interface for throughput intensive consumer electronics devices such as scanner, printers, mass storage devices, Cameras. IEEE1394 supports traditional asynchronous data transfers as well as isochronous data transfers.</p> <p>In order to solve this problem, better approach would be to process the image data as it is received by employing an field programmable gate array (FPGA), thus processing the algorithms using hardware.</p> | 2008 |

|     |        |  |   |      |
|-----|--------|--|---|------|
| 22. |        | Design of a lossless parallel high-speed data compression system                               | <p>The objective of the project is to design a lossless parallel data compression system which operates in high-speed to achieve high compression rate. By using Parallel architecture of compressors, the data compression rates are significantly improved. Also inherent scalability of parallel architecture is possible.</p> <p>The main parts of the system are the two Xmatchpro based data compressors in parallel and the control blocks providing control signals for the Data compressors, allowing appropriate control of the routing of data into and from the system.</p> | 2008 |
| 23. | ITVL23 | Reliable low power fir filter via reduced precision redundancy                                 | <p>In low-power application the main drawback is the increase in noise due to an error called soft error i.e. increase in critical path delay than the estimated one. Due to this error there is degradation in the performance of low power systems and there is a reduction in SNR than the system with normal supply voltage. Reduced Precision Redundancy PR) is a novel technique used to educe this so called soft error and maintaining the accuracy as well.</p>  | 2008 |
| 24. | ITVL24 | Design and implementation of low power pipelined FFT processor                                 | <p>The FFT processor is a critical block in all multi carrier systems used primarily in the mobile environment. The portability requirement of these systems is mainly responsible for the need of low power FFT architecture. This paper proposes a technique to reduce the power consumption of a popular low power radix- 4 pipelined FFT processor by modifying its operation sequence. The complex multiplier is one of the most power consuming blocks in the FFT processor.</p>  | 2008 |
| 25. | ITVL25 | Design and Implementation of Reversible Watermarking for JPEG2000 Compression Standard on FPGA | <p>With the result of advancement in today's technology, digital content can be easily copied, modified, or distributed. efficient watermarking algorithm has been implemented using Matlab which uses the concept of difference expansion of high pass transform coefficients with watermark bits. This work was to find a reversible watermarking algorithm for JPEG2000 standard for medical applications, a (5,3) wavelet transform is used which is considered as lossless transform in the JPEG2000 standard.</p>   | 2008 |



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|-----|--------|--|---|------|
| 26. | ITVL26 | A pipelined shared-memory architecture for FFT processor                               | This paper presented a VLSI architecture for the FFT processors-- which implemented the pipelined architecture to realize the high speed radix-2 Process Elements (PEs) and globally utilized the high-radix shared-memory architecture to implement the area-efficient FFT processors. Based on this architecture, a high performance 512-point FFT processor has been designed in the 0.6um 33v CMOS process to demonstrate its feasibility.  | 2008 |
| 27  | ITVL27 | FPGA implementation of USB transceiver Macro cell interface with usb2.0 specifications | The project deals with VHDL implementation of USB 2.0 Transceiver Macrocell Interface (UTMI) and testing the same by downloading it into FPGA (Spartan2). The Universal Serial Bus (USB) Transceiver Macrocell Interface (UTMI) is a two wire, bi-directional serial bus interface. The USB 2.0 specifications define three types of UTMI implementations depending on data transmission rates. These are<br>UTMI consists of transmission and receiving sections. The transmitter of the UTMI sends data to different USB devices through D+ and D- lines, where as, the receiver gets data on these same lines. | 2009 |
| 28  | ITVL28 | Vector signal analysis of digital baseband and if Signals within an FPGA               | Today all communication systems are prototyped on FPGAs before sending them for ASIC backend and fabrication. On other side the FPGAs with million gate logic density and embedded block RAMs allowed the high speed signal capturing and storage for real time analysis. There are several types of interface methods possible to communicate the FPGA with a computer. However UART being low weight and widely available in several FPGA boards it as an appropriate option for transferring the captured data   | 2009 |
| 29  | ITVL29 | GSM-Based Remote Sensing and Control System Using FPGA                                 | Home security today needs to make use of the latest available technological components. In this paper, we present the design and implementation of a remote sensing, control, and home security system based on GSM (Global System for Mobile). This system offers a complete, low cost, powerful and user friendly way of 24 hours real-time monitoring and remote control of a home security. The design has been described using VHDL (VHSIC Hardware Description Language) and implemented in hardware using FPGA (Field Programmable Gate Array).  | 2008 |

|           |               |   |  |      |
|-----------|---------------|---|--|------|
| <b>30</b> | <b>ITVL30</b> | An Accumulator-Based<br>Compaction Scheme<br>For Online BIST of RAMs            | Transparent built-in self test (BIST) schemes for RAM modules assure the preservation of the memory contents during periodic testing. Symmetric transparent BIST skips the signature prediction phase required in traditional transparent BIST schemes, achieving considerable reduction in test time. In symmetric transparent BIST schemes proposed to date, output data compaction is performed using either single-input or multipleinput shift registers whose characteristic polynomials are modified during testing. In this paper the utilization of accumulator modules for output data compaction in symmetric transparent BIST for RAMs is proposed. It is shown that in this way the hardware overhead, the complexity of the controller, and the aliasing probability are considerably reduced. | 2008 |
| <b>31</b> | <b>ITVL31</b> | A Compact AES Encryption<br>Core on<br>Xilinx FPGA                              | This paper presents an Advanced Encryption Standard (AES) encryption core on Field Programmable Gate Array (FPGA). The target device is Spartan-3 FPGA. We have designed an efficient and compact, iterative architecture with input and key, both of 128 bits. The throughput achieved is 2640.3712Mbps with a frequency of 206.28 MHz; using 8 embedded Block RAMs (DRAMs) and 390 Slices. The aim is to provide a fast encryption core for small size and low cost applications.  | 2009 |
| <b>32</b> | <b>ITVL32</b> | FPGA IMPLEMENTATION<br>FOR HUMIDITY AND<br>TEMPERATURE REMOTE<br>SENSING SYSTEM | Home security today needs to make use of the latest available technological components. In this paper, we present the design and implementation of a remote sensing, control, and home security system based on GSM (Global System for Mobile). This system offers a complete, low cost, powerful and user friendly way of 24 hours real-time monitoring and remote control of a home security. The design has been described using VHDL (VHSIC Hardware Description Language) and implemented in hardware using FPGA (Field Programmable Gate Array).   | 2008 |

|           |               |  |  |      |
|-----------|---------------|--|--|------|
| <b>33</b> | <b>ITVL33</b> | An improved RC6 algorithm with the same structure of encryption and decryption | In this paper, we propose an improved RC6 encryption algorithm that have the same structure of encryption and decryption. So far, conventional RC6 algorithms have difference structure of encryption and decryption. We devise our algorithm by inserting a symmetric layer using simple rotation and XOR operations, in which the half of whole RC6 rounds uses encryption procedure and the rest of it are employs decryption one.  | 2009 |
| <b>34</b> | <b>ITVL34</b> | VHDL Modeling of Wi-Fi MAC Layer for Transmitter                               | Wireless communication is one of the fastest growing technologies. The demand for connecting devices without cable is increasing everywhere. Wireless Local Area Networks (WLAN) can connect roaming devices to the Internet. At home, a wireless LAN can connect roaming devices to the internet. Wireless devices are both popular and cost effective and have considered interest from the industry and academia. Users of wireless networks either, walking on the streets, driving a car, or operating a portable computer on an aircraft, enjoy the exchange of information without worrying about how technology makes such exchange possible.                        | 2009 |
| <b>35</b> | <b>ITVL35</b> | A New Low Power Test Pattern Generator Using a Variable-Length Ring Counter    | A new built-in self-test (BIST) test pattern generator (TPG) for low power testing is presented in this paper. The principle of the proposed approach is to reconfigure the CUT's partial-acting-inputs into a short ring counter (RC), and keep the CUT's partial-freezing-inputs unchanged during testing. Experimental results based on ISCAS'85 and ISCAS'89 benchmark circuits show that 17% reductions in the test data storage, 43% reductions in the number of test pattern, 30% reductions in the average power, 19% reductions in the average power and 46% reductions in the total power consumption are attained during testing with a small size decoding logic | 2009 |

**DOMAIN: CORE VLSI**

| S.NO | PROJECT CODE | PROJECT TITLES  | DESCRIPTION   | YEAR |
|------|--------------|---|---|------|
| 36   | ITVL36       | On Clustering of Undetectable Single Stuck-At Faults and Test Quality in Full-Scan Circuits | In this paper, We describe an extension to the set of target faults ,the extended set of target faults consists of double stuck-at faults that include an undetectable fault as one of their components.  | 2010 |
| 37   | ITVL37       | Asynchronous Data-Driven Circuit Synthesis  | This paper is described for synthesizing asynchronous circuits based on the Handshake Circuit paradigm but employing a data-driven, rather than a control-driven, style.  | 2010 |
| 38   | ITVL38       | A Multibank Memory-Based VLSI Architecture of DVB Symbol Deinterleaver                      | In this paper, an efficient symbol-deinterleaver architecture compliant with the digital-video-broadcasting (DVB) standard is proposed.   | 2010 |
| 39   | ITVL39       | Implementation of a Self-Motivated Arbitration Scheme for the Multilayer AHB Busmatrix      | In this paper, we propose the design and implementation of a flexible arbiter for the ML-AHB busmatrix to support three priority policies—fixed priority, round robin, and dynamic priority and three data multiplexing modes—transfer, transaction, and desired transfer length. | 2010 |
| 40   | ITVL40       | A Galois field-based logic synthesis with testability                                       | In this paper introduces the generalized theory and a new fast efficient graph-based decomposition technique for the functions over finite fields defined over the set $GF(N)$ .  | 2010 |

**TECHNOLOGY: VLSI****DOMAIN: CIRCUIT AND SYSTEM**

| S.NO | PROJECT CODE | PROJECT TITLES   | DESCRIPTION   | YEAR |
|------|--------------|--|---|------|
| 41   | ITVL41       | Low Complexity Digit Serial Systolic Montgomery Multipliers for Special Class of $GF(2^m)$ | This paper presents a digit serial systolic multiplication architecture for all-one polynomials (AOP) over $GF(2^m)$ for efficient implementation of Montgomery Multiplication (MM) | 2010 |

|    |        |  |   |      |
|----|--------|--|---|------|
|    |        |  | Algorithm suitable for cryptosystem.  |      |
| 42 | ITVL42 | LUT Optimization for Memory-Based Computation  | This paper presents LUT-based multiplier involves comparable area and time complexity for a word size of 8 bits, but for higher word sizes, it involves significantly less area and less multiplication time than the canonical-signed-digit (CSD)-based multipliers.   | 2010 |
| 43 | ITVL43 | New Approach to Look-Up-Table Design and Memory-Based Realization of FIR Digital Filter          | In this paper, we show that the look-up-table (LUT)-multiplier-based approach, where the memory elements store all the possible values of products of the filter coefficients could be an area-efficient alternative to DA-based design of FIR filter with the same throughput of implementation.                           | 2010 |
| 44 | ITVL44 | Improved Area-Efficient Weighted Modulo $2n + 1$ Adder Design With Simple Correction Schemes     | This paper presents adders that can produce modulo sums within the range $\{0, 2^n\}$ , which is more than the range $\{0, 2^n - 1\}$ produced by existing diminished-1 modulo $2n + 1$ adders  | 2010 |
| 45 | ITVL45 | Pseudorandom Bit Generation Using Coupled Congruential Generators                                | This paper proposes the generation of a pseudorandom bit sequence (PRBS) using a comparative linear congruential generator (CLCG) as follows. A bit "1" is output if the first linear congruential generator (LCG) produces an output that is greater than the output of the second LCG, and a bit "0" is output otherwise. | 2010 |
| 46 | ITVL46 | Field programmable gate array prototyping of end-around carry parallel prefix tree architectures | In this paper, complete designed EAC adders that can work independently as a regular adder is proposed and present a comparative study on different parallel prefix trees which are used in the design of our new EAC adder targeting fieldprogrammable gate array (FPGA) technology.                                       | 2010 |

**DOMAIN: IMAGE PROCESSING**

| S.NO | PROJECT CODE | PROJECT TITLES                         | DESCRIPTION   | YEAR |
|------|--------------|--|---|------|
| 47   | ITVL47       | On Reducing Scan Shift Activity at RTL | This paper proposes a DFT-based approach for reducing circuit switching activity during scan shift is proposed. Instead of inserting additional logic at the gate level that may introduce additional delay on critical paths, the proposed method modifies the design at the register transfer level (RTL) and uses the synthesis tools to automatically deal with timing analysis and optimization. | 2010 |

**TECHNOLOGY: VLSI****DOMAIN: COMMUNICATION**

| S.NO | PROJECT CODE | PROJECT TITLES  | DESCRIPTION  | YEAR |
|------|--------------|---|--|------|
| 48   | ITVL48       | New Architectural Design of CA-Based Codec                                | This paper proposes a codec which requires significantly less hardware and power for decoding compared to the existing techniques employed for Reed–Solomon (RS) Codes. Also it has been shown that the CA-based scheme can easily be extended for correcting more than two byte errors. | 2010 |
| 49   | ITVL49       | An Efficient 4-D 8PSK TCM Decoder Architecture                            | This paper presents an efficient architecture for a 4-D eight-phase-shift-keying trellis-coded-modulation (TCM) decoder. TCM encoders usually employ high rate convolutional codes that yield many more transition paths per state than low-rate codes do.                               | 2010 |
| 50   | ITVL50       | Design Space Exploration of Hard-Decision Viterbi Decoding: Algorithm and | This work analyzes the design complexity by applying most of the known VLSI implementation   | 2010 |

|  |  |                     |  |  |
|--|--|---------------------|--|--|
|  |  | VLSI Implementation | techniques for hard-decision Viterbi decoding to a different set of code parameters. The conclusions are based on real designs for which actual synthesis and layouts were obtained. |  |
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## IEEE-2010 PROJECTS

### CONTENTS

#### DSP DIP

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|         |  |   |      |
|---------|--|---|------|
| ITIMP01 | An Entropy Interpretation Of The Logarithmic Image Processing Model With Application To Contrast Enhancement | The contrast definition has been shown to be consistent with some important physical Laws and characteristics of human visual system. In this project, we establish an information-theoretic interpretation of the contrast definition.   | 2009 |
| ITIMP02 | Phase Adaptive Super Resolution Of Mammography Images Using Complex Wavelets                                 | The proposed method exploits the structural characteristics of breast tissues being imaged and produces higher resolution mammography images with sufficient visual Fidelity that fine image details can be discriminated more easily.  | 2009 |
| ITIMP03 | Image Quality Assessment Based On Multi-scale Geometric Analysis   | In this project, to target the problems in image quality assessment (IQA), we develop a novel framework for IQA to mimic the human Visual system (HVS) by incorporating the merits from multi-scale geometric analysis (MGA), contrast sensitivity function (CSF), and the Weber's law of just noticeable difference (JND). In the proposed framework, MGA is utilized to decompose images and then extract features to mimic the multi-channel structure of HVS. | 2009 |
| ITIMP04 | A Fast Multilevel Algorithm For Wavelet-Regularized Image Restoration  | This project is a multilevel extension of the popular "Thresholded Landweber" algorithm for wavelet-regularized Image restoration that yields an order of magnitude speed improvement over the standard fixed-scale implementation. The Method is generic and targeted towards large-scale linear inverse problems, such as 3-D de-   | 2009 |

|         |   |  |      |
|---------|---|--|------|
|         |   | convolution microscopy.  |      |
| ITIMP05 | Low Bit-Rate Image Compression Via Adaptive Down-sampling And Constrained Least Squares Up-conversion                     | In this project, we propose a practical approach of uniform down sampling in image space and yet making the sampling adaptive by spatially varying, directional low-pass pre-filtering. The resulting down-sampled pre-filtered image remains a conventional square sample grid, and, thus, it can be compressed and transmitted without any change to current image coding standards and systems. | 2009 |
| ITIMP06 | Digital Image Watermarking and recovery of the secret image   | Using DWT we hide and recover a secret data in the low frequency Domain of the Image.  | 2008 |
| ITIMP07 | Image retrieval using Color, Texture and Shape  | The uniqueness of an image is checked and retrieved using Color, Texture and Shape using MATLAB  | 2008 |
| ITIMP08 | Face Detection Using Adaboost algorithm   | The face region of 'n' number of persons in an image is detected which will be useful in forensic department.  | 2008 |
| ITDSP09 | Analysis of Emotionally Salient Aspects of Fundamental Frequency for Emotion Detection                                    | This project presents an analysis of the statistics derived from the pitch contour. The results indicate that gross pitch contour statistics such as mean, maximum, minimum, and range are more emotionally prominent than features describing the pitch shape.  | 2009 |
| ITDSP10 | Efficient Convex Relaxation Methods for Robust Target Localization by a Sensor Network Using Time Differences of Arrivals | In this project, we consider the maximum likelihood formulation of this time difference of arrival (TDOA) target localization problem and provide efficient convex relaxations for this non-convex optimization problem.   | 2009 |
| ITDSP11 | A new delay less sub-band Adaptive filtering algorithm for active noise control systems                                   | In this project, we propose a new uniform-discrete Fourier transform (DFT) -modulated (UDFTM)-based adaptive sub-band filtering method that alleviates the degrading effects of the delay and side-lobe distortion introduced by the prototype filter on the system performance.   | 2009 |
| ITDSP12 | An ensemble speaker and speaking environment modeling approach to robust speech recognition                               | In this project we propose an ensemble speaker and speaking environment modeling (ESSEM) approach to characterizing environments in order to enhance performance robustness of automatic speech recognition systems under adverse  | 2009 |



|         |  |   |      |
|---------|--|---|------|
|         |  | conditions.   |      |
| ITDSP13 | Sampling theorems for signals from the union of finite-dimensional linear subspaces              | In this project, we consider a more general signal model and assume signals that live on or close to the union of linear Sub spaces of low dimension. We present sampling theorems for this model that are in the same spirit as the Nyquist Shannon sampling theorem in that they connect the number of required samples to certain model parameters.  | 2009 |
| ITCM14  | Communication Coverage In Wireless Passive Sensor Networks                                       | In this project, RF communication coverage in wireless passive sensor networks WPSN is analytically investigated. The required number of RF sources to obtain interference-free communication connectivity with the WPSN nodes is determined and analyzed in terms of output power and the transmission frequency of RF sources, network size, RF source and WPSN node characteristics.   | 2009 |
| ITCM15  | Channel coding for high-speed links: a systematic Look at code performance and system simulation | This project provides a deeper insight into joint error behaviors in high-speed links, extends the range of statistical simulation for coded high-speed links, and provides a case against the use of biased Monte Carlo methods in this setting. Finally, based on a hardware test bed, the performance of standard binary forward error correction and error detection schemes is evaluated, from which recommendations on coding for high-speed links are derived. | 2009 |
| ITCM16  | Training design for repetitive-slot-based CFO estimation in OFDM                                 | The proposed power loading schemes consist of allocating more power to activated carriers with higher signal-to-noise ratios. Simulation-based performance results of the maximum likelihood estimator support the Cramér-Rao bound CRB-based theoretical results.  | 2009 |
| ITCM17  | Efficient detection ordering scheme for MIMO Transmission using power control                    | In this project, an efficient ordering scheme for an ordered successive interference cancellation detector is determined under the bit error rate minimization criterion for multiple antenna systems using transmission power control.   | 2009 |
| ITCM18  | Finite-precision analysis of de-mappers and decoders For DPC-coded m-QAM systems                 | This paper discusses the choice of suitable quantization characteristics for both the decoder messages and the received samples in LDPC-coded systems using -QAM schemes. The analysis involves also the de-mapper block, that provides initial likelihood values for the decoder,  | 2009 |

|         |  |  |      |
|---------|--|--|------|
|         |  | by relating its quantization strategy with that of the decoder.  |      |
| ITDSP19 | Bandpass Sigma-Delta Modulator for Sensor Signal Processing                | This paper presents a system architecture for sensor signal digitization utilizing a bandpass sigma-delta modulator. The first version of the proposed system Architecture was implemented in 5V 0.7 $\mu$ m CMOS technology. The first version of the proposed system architecture is useful for our capacitive pressure sensor measurement. The paper describes the possibilities of using the proposed enhanced system architecture in impedance spectroscopy and in capacitive pressure sensor measurement. The bandpass sigma-delta modulators are well suited for wireless applications. This paper shows another way how to use its advantages. | 2009 |
| ITDSP20 | Effective Process of Signaling Information for Digital Broadcast Recording | Signaling information is defined as stream element that indicates events for interactive service. Careful management of signaling information is essential to accomplish satisfying level of interactivity while watching recorded content. For that purpose we propose a scheme to store and utilize signaling information efficiently.   | 2009 |

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